providing the microstructures in layers to be integrated in a substrate, wherein the passive matrix array on each of the plurality of microstructures is electrically connected to a respective drain wiring.

REMARKS

Claims 1-25 are pending. Claims 7, 11 and 17 have been withdrawn from consideration. By this Amendment, claims 1-3, 8-10, 12-14, 18 and 19 are amended; and Figures 24, 25 and 26A-26C are corrected by the attached Letter to the Official Draftsperson. Reconsideration based on the following remarks is respectfully requested.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

Entry of the amendments is proper under 37 CFR §1.116 since the amendments: (a) place the application in condition for allowance (for the reasons discussed herein); (b) do not raise any new issue requiring further search and/or consideration (since the amendments amplify issues previously discussed throughout prosecution); (c) do not present any additional claims without canceling a corresponding number of finally rejected claims; and (d) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented because they are made in response to arguments raised in the final rejection. Entry of the amendments is thus respectfully requested.

I. THE APPROVED DRAWINGS ARE CORRECTED

The Office Action approves the proposed drawing corrections and requires corrected drawings in reply to the Office Action. In response, corrected Figures 24, 25 and 26A-26C are submitted in the attached Letter to the Official Draftsperson.

II. THE CLAIMS DEFINE PATENTABLE SUBJECT MATTER

The Office Action rejects claims 1-6, 8-10, 12-16 and 18-25 under 35 U.S.C. §103(a) over U.S. Patent No. 5,824,186 to Smith et al. in view of the specification disclosure at paragraphs 9-11. This rejection is respectfully traversed.

Smith et al. does not teach, disclose or suggest "a passive matrix array that includes memory cells formed of ferroelectric capacitors, ... and a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array, the peripheral circuit being separately formed on the substrate, wherein the passive matrix array is electrically connected to the line driver circuit," as recited in claim 1, and as similarly recited in claims 2-3, 8-10, 12-14 and 18; and "separately forming the passive matrix array on each of a plurality of microstructures and providing the microstructures in layers to be integrated in a substrate, wherein the passive matrix array on each of the plurality of microstructures is electrically connected to a respective drain wiring," as recited in claim 19.

Instead, Smith et al. merely discloses microstructures self-aligning into recessed regions located on a substrate, particularly by a fluid slush to transport and dispense the microstructures.

The applicants' specification at paragraphs 9-11 do not make up for these deficiencies. Instead, the description of related art at paragraphs 9-11 particularly describes the related problem of a transistor deterioration due to high temperature formation of a ferroelectric film, and the problem of a ferroelectric film diffusion into the transistor region in the case of integrating the passive matrix array and the peripheral circuits on a single substrate. These paragraphs do not teach, disclose or suggest the claimed features as above recited.

Furthermore, the Office Action's asserted motivation to combine the disclosure at paragraphs 9-11 with the microstructure techniques taught by Smith et al. for the purpose of obviating the device performance drawbacks is derived from the applicants' own disclosure

resulting in improper hindsight reasoning. The Office Action has failed to bear its burden of a prima facie case of obviousness by its assertion that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have grown the conventional FEPMA and peripheral circuits separately and integrate them onto a common substrate through the microstructure techniques taught by Smith et al. for the purpose of obviating the device performance drawbacks as disclosed. None of the applied references, individually or in combination, teach, disclose or suggest separate formations and integration of a ferroelectric passive matrix array and a peripheral circuit, wherein the passive matrix array is electrically connected.

Even if combined, Smith et al. does not teach, disclose or suggest the passive matrix array being electrically connected to complete the integration. Rather, Smith et al. merely suggests slurry flotation and self-alignment into substrate recesses.

For at least these reasons, it is respectfully submitted that claims 1-3, 8-10, 12-14, 18 and 19 are patentable over the applied references. The dependent claims are likewise patentable over the applied references for at least the reasons discussed as well as for the additional features they recite. Applicants respectfully request that the rejection under 35 U.S.C. §103 be withdrawn.

III. CONCLUSION

In view of the foregoing amendments and remarks, Applicants submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1 - 25 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Richard J. Kim
Registration No. 48,360

JAO:RJK/dap

Attachments:
Appendix
Letter to the Official Draftsperson

Date: May 29, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Claims:

The following is a marked-up version of the amended claims:

1. (Three Times Amended) A ferroelectric memory, comprising:

a microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the microstructure;

a substrate, the microstructure being centrally positioned and integrated on the substrate; and

a peripheral circuit ~~for~~ comprising a line driver circuit peripheral to the passive matrix array, the peripheral circuit being separately formed on the substrate, wherein the passive matrix array is electrically connected to the line driver circuit.

2. (Three Times Amended) A ferroelectric memory, comprising:

a substrate;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the substrate;

a microstructure; and

a peripheral circuit ~~for~~ comprising a line driver circuit for the passive matrix array, the peripheral circuit being separately formed on the microstructure, the microstructure being peripherally positioned and integrated on the substrate, wherein the passive matrix array is electrically connected to the line driver circuit.

3. (Three Times Amended) A ferroelectric memory, comprising:

a first microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the first microstructure;

a second microstructure;

a peripheral circuit comprising a line driver circuit for the passive matrix array, the peripheral circuit being separately formed on the second microstructure; and

a substrate, the first and second microstructures being integrated on the substrate, wherein the line driver circuit is peripherally positioned and electrically connected with the passive matrix array.

8. (Three Times Amended) A ferroelectric memory, comprising:

a passive matrix array that includes memory cells formed of ferroelectric capacitors;

a peripheral circuit comprising a line driver circuit for the passive matrix array;

an associated circuit having a same or a different function as the memory cells;

a single substrate; and

a plurality of microstructures, the passive matrix array, the peripheral circuit and the associated circuit being separately formed on each of the plurality of microstructures, the microstructures being integrated on the single substrate, wherein the line driver circuit is positioned and electrically connected with the passive matrix array.

9. (Three Times Amended) A ferroelectric memory, comprising:

a passive matrix array that includes memory cells formed of ferroelectric capacitors;

a peripheral circuit comprising a line driver for the passive matrix array; and

a single microstructure, the passive matrix array and the peripheral circuit being separately fabricated, positioned and integrated on the single microstructure, wherein

the line driver circuit is peripherally positioned and electrically connected with the passive matrix array.

10. (Three Times Amended) A ferroelectric memory, comprising:

a first microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the first microstructure;

a second microstructure that is larger than the first microstructure, the first microstructure being provided in a central part of the second microstructure to be integrated; and

a peripheral circuit ~~for~~ comprising a line driver circuit peripheral to the passive matrix array, the peripheral circuit being separately formed on the second microstructure, wherein the line driver circuit is electrically connected with the passive matrix array.

12. (Three Times Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit ~~for~~ comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

forming the passive matrix array on a microstructure;

separately forming the peripheral circuit on a substrate; and

centrally positioning and integrating the microstructure on the substrate, wherein the passive matrix array is electrically connected to the line driver circuit.

13. (Three Times Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit ~~for~~ comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

forming the passive matrix array centrally disposed on a substrate;

separately forming the peripheral circuit on a microstructure; and

integrating the microstructure on the substrate, wherein the line driver circuit is peripherally positioned and electrically connected with the passive matrix array.

14. (Three Times Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit ~~for~~ comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

forming the passive matrix array on a first microstructure;

separately forming the peripheral circuit on a second microstructure; and

integrating the first and second microstructures on a substrate, wherein the line driver circuit is peripherally positioned and electrically connected with the passive matrix array.

18. (Three Times Amended) A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit ~~for~~ comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

forming the passive matrix array on a first microstructure;

separately forming the peripheral circuit on a second microstructure which is larger than the first microstructure; and

providing the first microstructure in a central part of the second microstructure to be integrated, wherein the line driver circuit is electrically connected with the passive matrix array.

19. (Three Times Amended) A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric

capacitors, and a peripheral circuit ~~for~~ comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

separately forming the passive matrix array on each of a plurality of microstructures; and

providing the microstructures in layers to be integrated in a substrate, wherein the passive matrix array on each of the plurality of microstructures is electrically connected to a respective drain wiring.